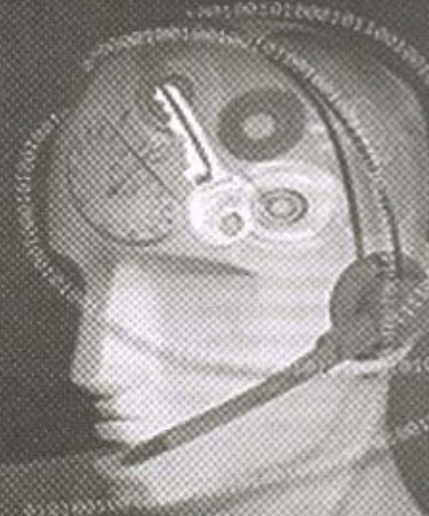


Admission open for

# VLSI Designing



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- Introduction to VLSI designing.
- Video and Presentation regarding history and current trends.
- Overview of transistors (BJT and FET).
- Simulation in PSpice.
- Advantages of FET over BJT in VLSI Designing.
- PSpice simulation exercises and assignments.
- Overview of basic gates.
- Introduction to DSCH3.
- Practice of basic gate simulations in DSCH3.
- KMap SOP and POS simplification.
- NAND and NOR Logic.
- Simulation of above concepts in DSCH3.
- Create Adder, Multiplexer, Comparator, Encoder and Decoder.
- Overview of latches and flipflops.
- Creation of flip flops in DSCH3.
- Creating custom symbols in DSCH3 and Block level design.
- Design and simulation of counters and shift registers.
- CMOS architecture and working.
- Pull up/Pull down network concept.
- CMOS level design of following:
  - Inverter
  - Nand Gate
  - The NOR Gate
  - Compound Gates
  - Pass transistors and Transmission Gates
  - Tristates
  - Multiplexers
  - Latches
- Flip-flops
  - CMOS fabrication and layout concepts.
  - Introduction to MICROWIND.
  - Design of basic gates using MICROWIND.
  - 3D step by step analysis of manufacturing process.
  - Timing analysis of MOS Designs in MICROWIND.
  - Introduction to verilog language.
  - Quicker MOS Design using verilog in MICROWIND.
  - Introduction to XILINX.
  - Concepts of VHDL
    - Abstraction
    - Behavioural Description in VHDL
    - RT Level in VHDL
    - Gate Level in VHDL
  - Introduction to VHDL Coding in XILINX
  - VHDL Language and Syntax
  - Verilog Language and Syntax:
  - Schematic design on Altera.
  - Testbench simulation on Altera.
  - Verilog and VHDL coding in Altera.
  - Downloading and testing on VLSI Protoboard
  - Microcontroller Systems.
  - AVR GCC.
  - Familiarity with AVR Studio.
  - Downloading and testing on stk500.
- VHDL module coverage:
  - Access type
  - Aggregate
  - Alias
  - Allocator
  - Architecture
  - Array

- Assertion Statement
- Attributes (predefined)
- Attributes (user defined)
- Bit
- Bit\_vector
- Block statement
- Boolean
- Case statement
- Character type
- Component declaration
- Component instantiation
- Composite type
- Concatenation
- Configuration declaration
- Configuration specification
- Constant
- Delay
- Driver
- Entity
- Enumeration type
- Event
- Exit statement
- Expression
- File type
- Floating point type
- Function
- Generate statement
- Generic
- Group
- Guard
- Identifier
- If statement
- Integer type
- Library clause
- Literal
- Loop statement
- Name
- Next statement
- Null statement
- Operator overloading
- Operators
- Package
- Package body
- Physical type
- Port

- Procedure
- Process statement
- Range
- Record type
- Report statement
- Reserved word
- Resolution function
- Resume
- Return statement
- Scalar type
- Sensitivity list
- Signal assignment
- Signal declaration
- Slice
- Standard package
- Std\_logic
- Std\_logic\_1164 package
- Std\_logic\_vector
- String
- Subtype
- Suspend
- Testbench
- Type
- Type conversion
- Use clause
- Variable assignment
- Variable declaration
- Vector
- Vital
- Wait statement
- Waveform

VERILOG module coverage:

- Always procedural block
- Arithmetic operators
- Arrays
- Bit-select
- Blocking assignment
- Block statement
- Case statement
- Comment
- Concatenation
- Conditional operators
- Continuous assignments
- Data types

- Delays
- Disable statement
- Equality operators
- Events
- Expressions
- For loop
- Forever loops
- Function
- Gates
- Identifier
- If statement
- Initial procedural blocks
- Integer data types
- Integer numbers
- Logical operators
- Logic strength
- Logic values
- Module definition
- Module instances
- Module ports
- Net data types
- Non blocking data types
- Number representation
- Operators
- Parameters
- Part select
- Port connections
- Primitives
- Primitive instances
- Procedural assignments
- Procedural blocks
- Real data type
- Real numbers
- Reduction operators
- Register data types
- Relational operators
- Repeat loop
- Reserved keywords
- Shift operators
- String data type
- System task and functions
- Task time data type
- User defined primitive
- Vector
- Wait statement
- While loop

